The Phase 2 Upgrade of the CMS Inner Tracker

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The Phase 2 Upgrade of the CMS Inner Tracker

S. Orfanelli for the CMS collaboration

CERN, Espl. des Particules 1, Geneva, Switzerland

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ABSTRACT

A new silicon tracker will be built for the Phase 2 Upgrade of the CMS experiment to fully exploit the increased luminosity delivered by the HL-LHC. The innermost part, called the Inner Tracker, will be exposed to extreme conditions such as unprecedented radiation levels of 1.2 Grad and 2.3×10^{16} n_{eq}/cm^2 and hit rate of 3.2 GHz/cm^2. The new Inner Tracker relies on many novel solutions and technologies that allow for a design of a light and radiation-hard pixel detector of high performance. The hybrid pixel modules will be composed of pixel sensors with pixel size of 2500 μm^2 and a new ASIC, designed in 65 nm CMOS technology, developed by the RD53 collaboration. A novel scheme of serial powering will be deployed to power the pixel modules and new technologies will be used for a high bandwidth readout system. The mechanics will be lightweight, based on carbon-fibre material and two-phase CO_2 cooling. In this contribution, the design of the CMS Inner Tracker system will be presented along with the prospective design choices.

1. Motivation and introduction to the CMS Inner Tracker

Motivation. After the end of Long-Shutdown 3, the LHC will be entering the new High-Luminosity (HL) phase, reaching 5 to 7 times its nominal luminosity. According to the latest schedule, announced at the end of 2019, the operation of the accelerator will be resumed in 2027 and will reach a peak instantaneous luminosity of 7.5×10^{34} cm^{-2} s^{-1} and an integrated luminosity of 3000 fb^{-1} by the end of ten years of operation. The increased luminosity will be accompanied by a significant increase in the number of pile-up events per collision (up to 200), five times higher than the current value of ∼40 (in 2018). In addition to the increased hit rate leading to higher detector occupancy, the radiation that the detector parts will be exposed to will reach unprecedented levels. The CMS experiment will undergo a major upgrade during Long-Shutdown 3 to be able to fully exploit the physics potential during the HL-LHC era. This upgrade is commonly referred to as the Phase 2 upgrade.

The CMS Tracker is the system located in the heart of the CMS detector and exposed to the most harsh operational conditions. A complete new Tracker will be built for the Phase 2 upgrade aiming to maintain and even improve the tracking performance compared to its predecessor [1]. It will be fully built by hybrid silicon modules i.e. silicon sensors readout by ASICs. The detector system is divided into two subsystems, the Outer Tracker (OT) [2], that is based on silicon strips and macro-pixels, and the Inner Tracker (IT), that is exclusively using pixelated sensors. The new pixel detector will need to withstand up to 1.2 Grad of Total Ionising Dose (TID) and a hadron fluence of 2.3×10^{16} n_{eq}/cm^2 and cope with hit rates of up to 3.2 GHz/cm^2 for the innermost layer (30 mm from the beam line), a trigger latency of 12.8 μs and a trigger rate of 750 kHz. These requirements pose significant challenges for the design of the IT system to deliver the required physics performance.

CMS Inner Tracker. The new IT system has increased its granularity and will be composed of ∼2 billion pixels of 2500 μm^2, readout by a newly developed highly performant chip of similar cell size. In addition, the layout of the detector has been extended to cover the pseudorapidity region up to $|\eta| = 4$, which plays an important role in the improvement of the overall CMS physics performance by increasing the b-tagging efficiency of forward jets [3]. Innovative technology choices including light mechanical structures, cooling and powering solutions are deployed, such that a low material budget is achieved without compromising the tracking and vertexing capability of the system.

The most recent layout of the CMS Inner Tracker is shown in Fig. 1. The barrel part of the detector, known as TBPX, will be made out of four cylindrical layers, each 400 mm long, with the innermost located only 30 mm away from the beam line. The TBPX is split into two quasi-equal halves, with four and five module per end, in order to avoid a projective gap at $|\eta| = 0$. The structures where the modules are mounted are called “ladders". Eight small disks per end, with four rings of modules each, will compose the forward part of the detector (TFPX), while the extension to pseudorapidity of $|\eta| = 4$ will be built with four large disks per end, with five rings each (TEPX). There are two types of modules that will be used in this layout; the two inner layers of the TBPX and the two inner rings of TFPX disks will be double-chip modules (shown in green in Fig. 1), while the two outer layers of TBPX, the outer rings of TFPX and TEPX will be based on quad-chip modules (shown in yellow in Fig. 1).

E-mail address: styliani.orfanelli@cern.ch.

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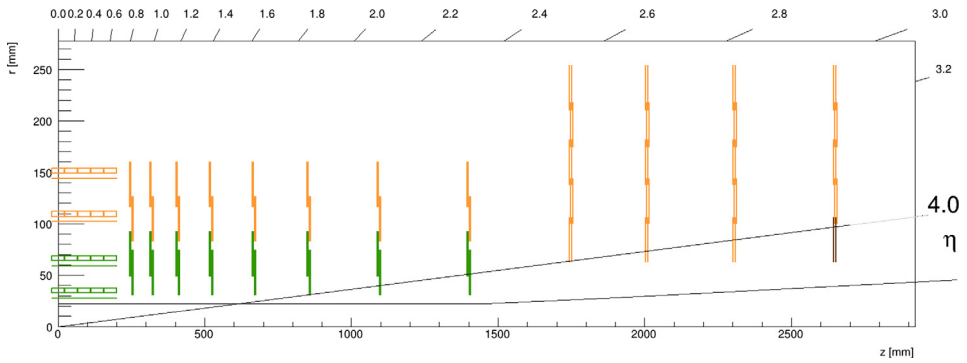

Fig. 1. The layout of the CMS Inner Tracker. (For interpretation of the references to colour in this figure legend, the reader is referred to the web version of this article.)

The entire TEPX will have an additional functionality, since it will be operated as a large powerful luminometer. The modules of TEPX will receive extra triggers and collect data for luminosity measurements. Moreover, the innermost ring of the last disk of TEPX will be exclusively dedicated to luminosity and background monitoring and will have independent readout and control (shown in brown in Fig. 1).

As shown in Fig. 2, the detector layout will be relatively simple, without any modules tilted or arranged in a turbine-like geometry. Power, cooling, and data transmission services will be carried on a cylindrical shell enclosing the pixel detector called the service cylinder and will be independent for each quarter of the detector (Z+/Z- and X+/X-). A simple installation and removal scheme is supported as the detector needs to be removed during each long shutdown giving also the possibility to replace and repair parts, if needed.

2. Pixel module components

Module. The IT modules have a relatively simple design. A High-Density Interconnect (HDI) PCB is used to distribute data, commands and power to and from the modules. Fig. 3 shows the design of the HDI for the double-chip (left) and quad-chip modules (right) [4]. The chips of a module are bump-bonded to the silicon sensor (shown in turquoise) which will be glued to the HDI (shown in green). The chips are the only active components on the module, which will be mounted with aluminium nitride rails on the cooling pipes. The chips are wire-bonded via the pad-frame (shown in light blue) to the HDI. The HDI features a flexible pigtail for the power connection and has mounted on it passive components, such as decoupling capacitors and external resistors used for setting some of the chip operational parameters such as the reference current I_{ref}, as well as power and readout connectors (shown in grey).

Sensor. An intensive R&D effort is ongoing for the development of radiation-hard small-pitch pixel sensors. Achieving high efficiencies for fluences higher than $1.0 \times 10^{16}\,n_{eq}/cm^2$ levels is challenging and requires an equally radiation hard ASIC to readout the sensor. The arrival of the pixel ASIC demonstrator [5] developed by the RD53 collaboration has enabled a long test-beam campaign to qualify pixel sensors for CMS. Special light-carrier boards hosting single-chip pixel modules with minimised material have been developed and allows an easy handling of irradiated modules during these irradiations and test-beams. The aspect ratio of the pixel can be either square of $50 \times 50\,\mu m^2$ or rectangular, i.e. $25 \times 100\,\mu m^2$. The readout ASIC has a cell size of $50 \times 50\,\mu m^2$ and it can be used to test both pixel sensor aspect ratios with appropriate bump-bonding patterns.

Two options of sensor technology are being explored: thin planar sensors and 3D sensors, both of ~150 μm active thickness. The thin planar n-in-p sensors are the baseline choice for the CMS Inner Tracker outer layers and rings. They require high bias voltage (0.8–1.0 kV) for efficient charge collection after irradiation. Their development entails challenges such as achieving high efficiencies within limited space due to the sensors' structures which reduces their efficiency and the need of spark protection because of the high voltage at the periphery of the sensor close to the readout chip. At the end of 2019, CMS started exploring the option of parylene coating as a spark protection and a list of tests are planned for 2020 to verify its reliability after irradiation.

On the other hand, the 3D sensors look like the most promising option for locations where radiation hardness is of particular importance, since the impact of charge carrier trapping, a limiting factor for planar sensors at large fluences, is reduced. They require low bias (150 V) for efficient charge collection after irradiation. An additional advantage of this technology, which is important for the first layer of the barrel, is the small inactive edge of the sensor. Another difference with respect to the planar sensors is the larger cell capacitance (up to 50 fF) which is a source of noise for the front-end electronics. Although they are very appealing, the fact that their fabrication is complex makes them potential candidates only for locations that are exposed to the highest radiation levels (TBPX innermost layers and the innermost ring of TFPX).

The current status of this R&D is that planar sensors have been qualified to levels of $5.0 \times 10^{15}\,n_{eq}/cm^2$ (layer 2 fluence). These levels would allow them to be operated for full HL-LHC programme for the entire IT system except for the innermost layer and ring [6]. The 3D sensors, on the other hand, have been qualified to half the fluence of the TBPX innermost layer [7]. The next steps planned for 2020 are tests with sensors that will be irradiated to the ultimate levels of fluence of $2.3 \times 10^{16}\,n_{eq}/cm^2$. The final choice of sensor technology as well as the pixel aspect ratio are two important decisions that will be taken in 2020.

ASIC. A family of pixel readout chips is being developed by the RD53 collaboration for both the ATLAS and CMS pixel detectors. Each experiment will have its own flavour of the chip, tailored to its specific requirements. Nevertheless, the core development and the IP blocks used are common. The first chip developed was a demonstrator chip with half the size of the final pixel chips, known as RD53A.

The RD53A pixel matrix is composed of 192 × 400 pixels with $50 \times 50\,\mu m^2$ size. The area of each pixel is 50% dedicated to the analogue and 50% to the digital part. The matrix is built up of 8 × 8 pixel cores where each core is made of 16 analogue "islands" (2 × 2 quads) embedded in a flat digital synthesised sea, as shown in Fig. 4. A pixel core can be simulated at transistor level with analogue simulator tools.

Three Analogue Front Ends (AFE) have been integrated in RD53A for performance comparisons within the same layout area. They were identified by their names: Synchronous FE, the Linear FE and the Differential FE. All of them were designed for low power (~5 μA/pixel), low threshold operation (below 1000 $e-$), low level of fake rate (<1e-6 per chip) and were compatible with the sensor capacitance (50 fF) and increased leakage currents after irradiation (up to 10 nA per pixel). The digital logic for signal digitisation, storage, trigger-matching and readout are shared among several pixels, called Pixel Regions. Two

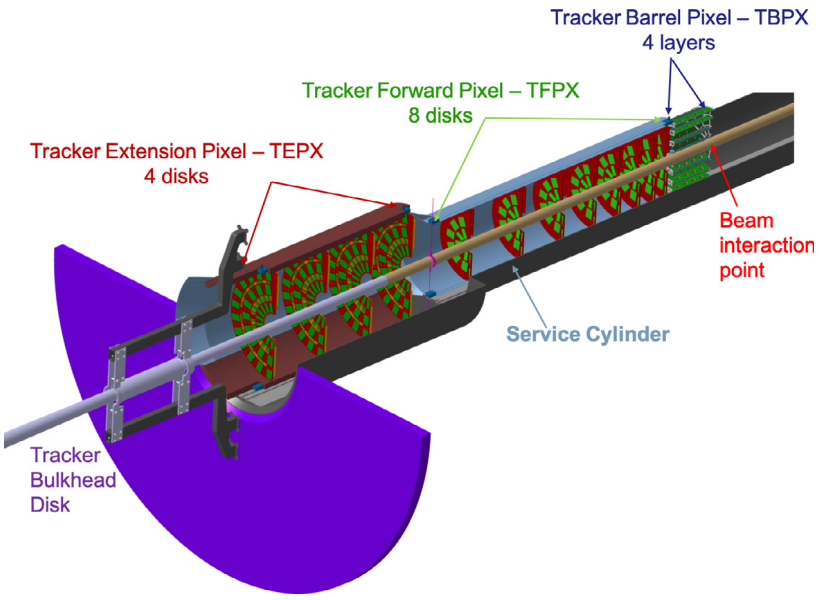

Fig. 2. A quarter of the IT system.

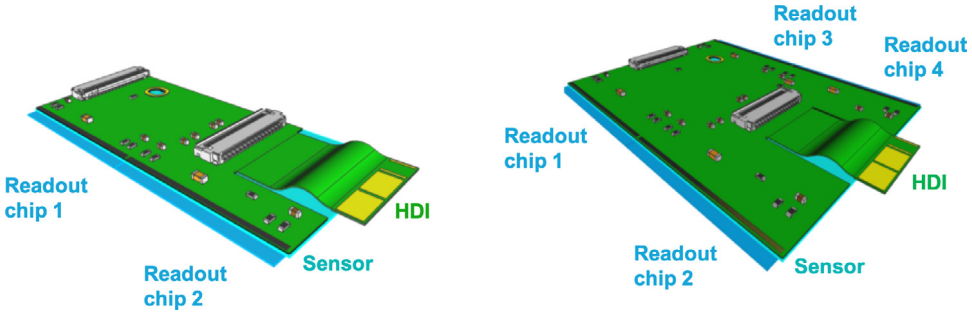

Fig. 3. The 1 × 2 (left) and 2 × 2 (right) module design for the CMS IT system. (For interpretation of the references to colour in this figure legend, the reader is referred to the web version of this article.)

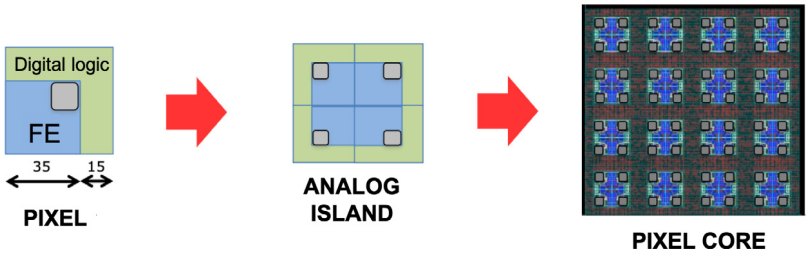

Fig. 4. Pixel cores are composed of 16 analogue "islands" embedded in a digital "sea".

digital readout architectures were implemented in RD53A to explore two approaches on buffering resources shared in a limited pixel area, both allowing to run at high hit rate (3 GHz/cm^2), high trigger rate (1 MHz) long latencies (12.8 μs) with < 1% inefficiency. The RD53A was designed to be radiation hard up to 500 Mrad. The chip periphery located at the bottom of the chip contains Shunt-LDO regulators [8] that enable the serial powering of the pixel modules, four fast (1.28 Gbps) data output links using the Aurora protocol [9], a 160 Mbps control link and other digital and analogue circuitry needed to bias, configure and monitor the functionality of the chip.

The current status of the pixel ASIC development is that the chip has been extensively tested and proven to be fully functional, meeting specifications [10]. All AFE have demonstrated good performance after irradiation and have achieved a low operational threshold of 1000 $e-$. In 2019, after a very detailed review process, CMS has chosen the flavour of the front-end for the implementation in the final pixel chip to be the Linear Front-End [11]. The common design framework of the final pixel ASIC, known as RD53B, contains design improvements and few bug-fixes with respect to RD53A. The next steps for this critical IT system component is the submission of the final CMS pixel chip in 2020.

3. System design

3.1. Introduction

The pixel modules, described in the previous section, will be readout and controlled by electrical links (e-links). The electrical signals will be converted to optical in the optomodule of the system, known as the portcard. The role of the portcard is to host two LpGBT [12] chips

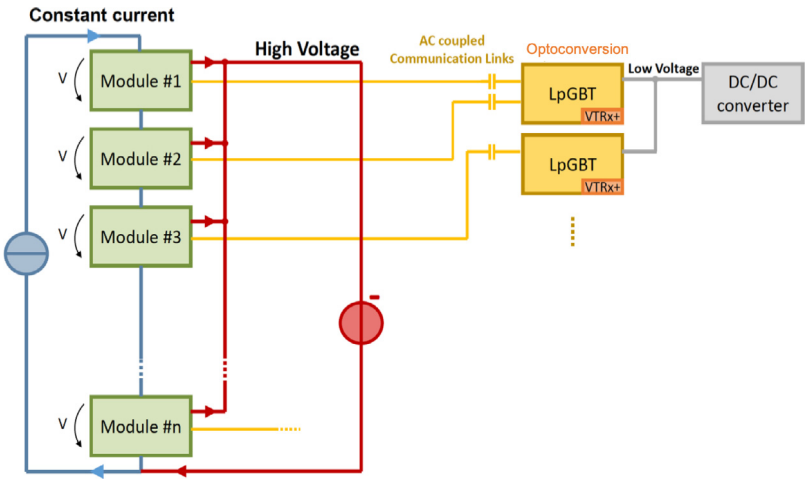

Fig. 5. IT system architecture, based on groups of serially powered modules.

together with two VTRx+ [13] and send the data via optical fibre at 10 Gbps to the back-end boards while receiving from them the command stream at 2.5 Gbps. The portcards will be powered independently by a two stage DC–DC converter scheme located on these boards. The portcards will be installed at locations in the outer radius of the system, since the optoelectronics have limited tolerance to radiation. For the entire IT system, around 11k e-links will be used to readout and control the 4k pixel modules with 750 portcards using 1.2k LpGBT chips.

An important aspect of the CMS IT design is the choice of serial powering scheme for the pixel modules [14]. The serial powering scheme dictates the grouping of the modules in serial power chains and no crossing of the readout or the sensor biasing is allowed among modules that belong to different chains (see Fig. 5). A portcard is allowed to readout only modules belonging to the same chain. Given that the modules' reference levels differ along the chain, the e-links are AC-coupled at both the module (command stream) and the portcard side (data stream).

The CMS IT system will be built with lightweight carbon-fibre/foam structures and will be cooled using low-mass CO_2 evaporative cooling. The high performance of the IT cooling is essential not only for the longevity of the sensors, but also for the radiation hardness of the readout chip.[1] The cooling pipes will be shared among neighbouring modules targeting to keep the sensors below −20 °C. Extensive finite element studies are done to optimise the cooling parameters.

3.2. Powering of the IT modules

The specifications for the future readout pixel chip impose the use of scaled CMOS technology, featuring low voltage supply to guarantee both the target resolution and a sustainable power density, while still allowing to implement the necessary functionalities. Each pixel chip will consume about ∼2 A and will need a supply voltage of 1.4–1.5 V. Around 50 kW will be required to be delivered to the Inner Tracker system to power the 4k pixel modules. Most of this power will be consumed by the ASICs. The use of DC–DC power conversion has been excluded due to radiation hardness and material budget reasons. Therefore, a serial power distribution system has been proposed to power the pixel modules.

This power scheme is radiation hard, based on an integrated on-chip solution and minimises the amount of cables in a detector targeting a low material budget. It relies on providing a constant current to the system which makes it a rather low noise powering scheme, insensitive to the activity of the chips as well as to voltage drops along the cables. In a serial powering scheme, a constant current is injected in a group of modules put in series and the current is fed from one module the next one via the HDI pigtail. The chips of a module are powered in parallel, which means that the current of a module gets shared among them. Two Shunt-LDO regulators located on the bottom of each chip provide independently the analogue and digital supply voltages to the chip core. Each one of the regulators can take 2 A as input current. The chip consumes the majority of the current provided to it according to its needs while any excess current gets shunted by the shunt part of the regulators. It is crucial for the stability of serial powering to always provide an extra current of about 20% to the chain, which is called *current headroom*. The power consumption of the chip at maximum hit and trigger rate, including any Shunt-LDO losses, is expected to be $<1\ W/cm^2$.

The segmentation of the CMS IT electronics system in serial power chains is fundamental to its design. The total number of serial power chains in the CMS IT system is 500, with an average length of 8 and a maximum of 12 modules per chain. In the barrel, a serial power chain will be composed of the modules of two adjacent ladders of a layer. Given that the ladders of a TBPX quarter are half-length (reaching up to Z=0) and each one will be carrying 4 or 5 modules, the number of modules in a barrel serial power chain will be 8 or 10 (depending on the Z+/Z- end). Fig. 6 shows a part of a serial power chain for the barrel (one ladder). In the case of the disks, the modules will be grouped in chains per ring. Each side of the disk (front/back) will have independent chains. Therefore, the length of a chain equals to the number of the modules of a ring mounted on one side of the disk, corresponding to a minimum of 5 (innermost ring of TFPX) and a maximum of 12 (outermost ring of TEPX).

The bias of the sensors will be applied in parallel along the modules of a chain with one or two lines, depending on the location. The bias voltage seen by each sensor will differ by the voltage drop along the chain (∼1.4 V–1.5 V), which means that each sensor will be biased with a different value of voltage. This difference should not be a problem for the planar sensors, which require high values of bias voltage. Nevertheless, it can become significant for the 3D sensors, which have lower depletion voltage. Therefore, it has been decided to use two sensor bias lines per chain in the TBPX.[2] A maximum number of five modules with 3D sensors would be biased in parallel with a maximum voltage difference of 5*1.5 V= 7.5 V, which is considered acceptable. For the disks, the granularity of the sensor bias is kept the same with the serial powering: one line will be used to bias in parallel the sensors of a serial power chain (from 5 up to 12 modules, depending on the ring).

[1] The 65 nm CMOS technology is proven to be sufficiently radiation hard only if irradiated cold (below −10 °C).

[2] Only the two inner layers of TBPX are candidates for 3D sensors, but for homogeneity the entire TBPX follows this scheme.

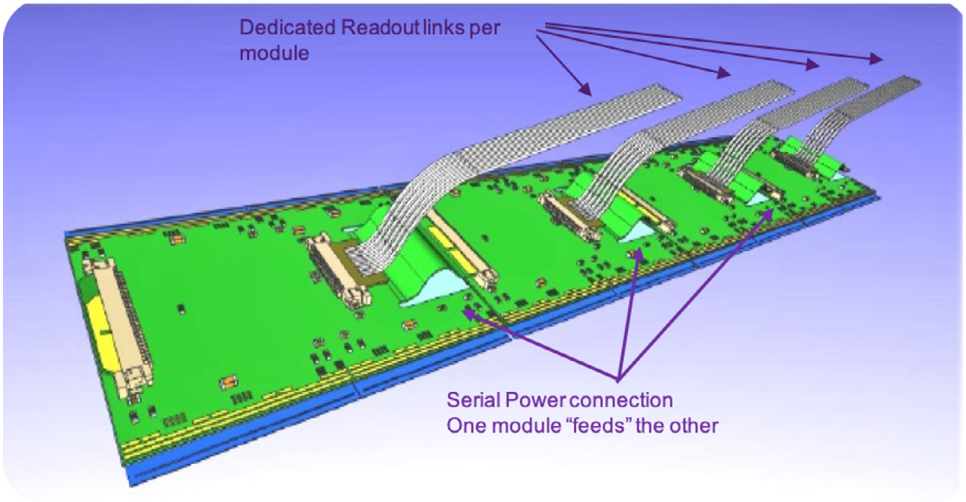

Fig. 6. Barrel modules of a ladder in a serial power chain.

This decision covers also the case of TFPX innermost ring, another candidate location for 3D sensors, since this ring and hence chain is only composed of 5 modules. The longest chain with planar sensors sharing the same bias line corresponds to the longest serial power chain of the system, the outermost ring of TEPX with 12 modules.

3.3. High bandwidth readout

The readout chain of the system is shown in Fig. 7. The first part of the data and command stream outside the modules are the e-links which connect the modules to the LpGBT chips on the portcards. The e-links used for the readout of the pixel chips will be running at 1.28 Gbps and will be carrying the data from L1 accept as well as monitoring information to the DAQ and control system. A 25% bandwidth headroom is reserved on the links. An efficient data formatting will be used in the chip in order to reduce the data rates by a factor of about 2. The modularity of the data links depends on the hit rate, i.e. the location of the modules they are reading out. The maximum number of data links per module is needed for the modules of barrel layer 1, where six links are needed. The minimum is one readout link per module for the outer layers and rings, where this link will be shared among the chips of a module, relying on a special data-merging functionality integrated on the chips.

The command links will be running from the LpGBT to the modules at 160 Mbps with a custom-made protocol developed for the control of RD53 chips. One control link will be used per module and will transmit clock, trigger, commands and configuration data to the chips. The second component of the portcards, the VTRx+, will be responsible for the electrical to optical conversion of the data with 10 Gbps rate and will receive the commands from the back-end boards at 5 Gbps. A dedicated IT Data Acquisition (DAQ) Interface board located at the service cavern, of ATCA format, called DTC (Data Trigger Control) will be used. A total of 28 of these boards will be needed for the entire CMS IT. Dedicated boards and crates will be used for the luminosity and background measurements exploiting TEPX.

4. System development

4.1. Component development

Many developments took place in 2019 for the IT system. The first version of the HDI was made available and was found to be fully operational. It was designed for quad-chip modules and double-chip modules using RD53A chips without sensors (so called digital modules). This development included the design of the assembly tools and establishing the assembly procedures. A fully assembled RD53A quad-chip digital module is shown in Fig. 8 (left). Within 2020, pixel modules with sensors bump-bonded to RD53A chips will replace the digital modules and will enable more studies at system level.

Another important milestone achieved in 2019 is the arrival of a demo portcard shown in Fig. 8 (right). The demo portcard contains one pair of LpGBT and VTRx+ and has been tested together with prototype e-links. The size of the PCB is similar to the final one for a realistic check of layout, routing and space integration. It contains two connectors for connecting prototype electrical links but has also the option of coaxial connections for debugging purposes. For its first iteration a regulator on-board was used to power it. In 2020, a mezzanine board with the DC–DC converters will be used to power it as in the final system. So far, the portcard has been proven to be functional and it is currently being integrated into the system tests described in the following section.

The development of a DAQ for reading out and controlling the RD53A pixel modules has been essential for the development of the system and its testing. While the final DTC boards are still in the design phase, a version of the DAQ has been developed for the FC7 boards [15]. These are μTCA format boards, which are used for the data acquisition system of the current CMS pixel detector. Appropriate mezzanine boards and adapter boards have been designed and manufactured to connect to RD53A single chip cards, RD53A modules via commercial cables, prototype e-links and the demo portcards allowing to test both the electrical and the optical readout paths of the system.

4.2. System tests

Power. The first system tests of RD53A digital modules operated in serial power chains took place in 2019. The digital modules have been used to construct a serial power chain of four modules in a barrel (ladder) geometry as well as in a ring topology, both shown in Fig. 9 [16]. In the case of the ring, a special flex circuit with two 50 μm aluminium layers has been developed to carry the current from one module to the other. The two mechanical structures for these tests were made out of aluminium blocks that have a thin layer of aluminium nitride for electrical insulation. The modules were fixed on the structures with clamps and no additional thermal material was used between the aluminium and the chips. The dimensions of the flex were chosen such that it would fit in the final detector to power the ring with the most stringent space constraints, which is the innermost ring of TFPX. The measurements conducted on these structures have demonstrated the robustness of the serial powering scheme on system level. The next steps planned for the IT system tests are the replacement of the digital modules with sensors on realistic carbon-fibre structures for grounding and noise studies.

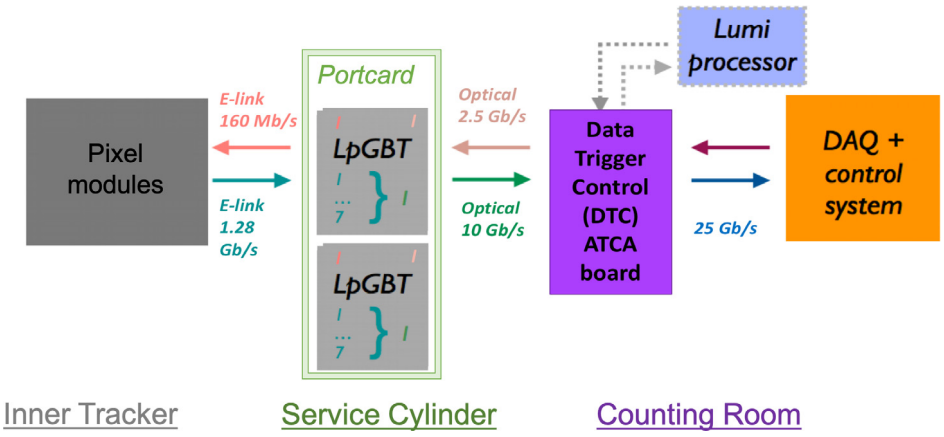

Fig. 7. IT system readout architecture.

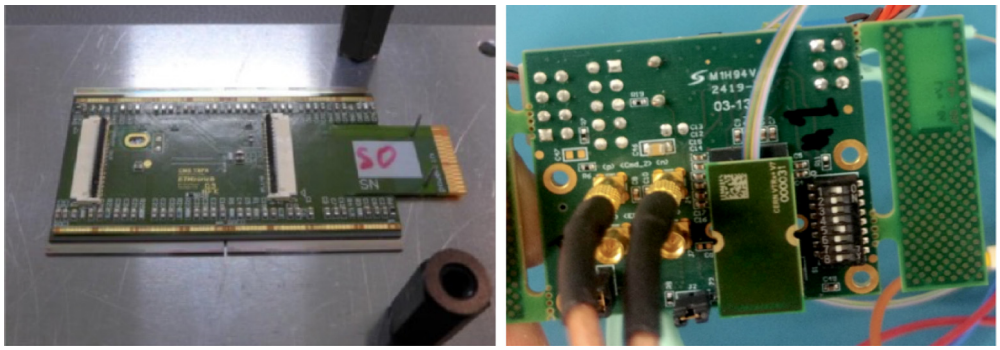

Fig. 8. A digital RD53A quad-chip module (left) and a demo portcard (right) with a fibre leaving VTRx+ and a LpGBT hidden below it.

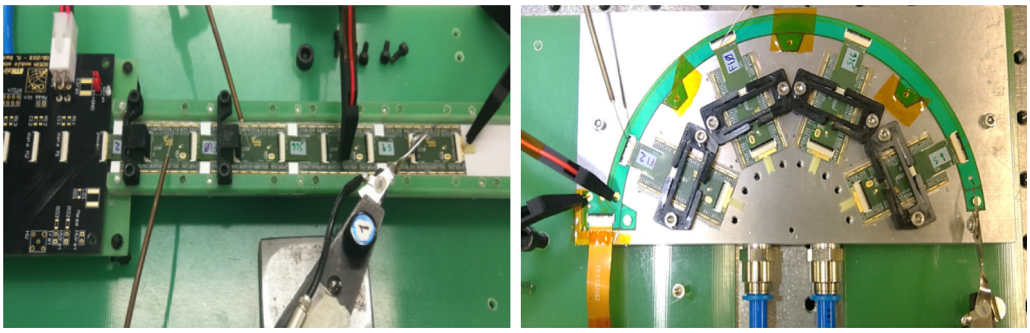

Fig. 9. The two system demonstrators for the barrel (left) and the ring (right) topologies.

Readout. There will be 7k readout and 4k control e-links used in the CMS IT system to connect the modules to the portcards. Currently two options of e-links are being explored. Twisted pairs of AWG36 or AWG34 are more suitable for the needs of the barrel because of their complex routing towards the portcards. A flex circuit option looks more suitable for the readout of the disks. The minimum length of the e-links in the system is around 35 cm and the longest is expected to be around 1.6 m. The objective of their development is to minimise their mass to acceptable cable losses while keeping the amplitude and the jitter within acceptable levels for the LpGBT. The pre-emphasis of the RD53 chip driver as well as the equalisation of the LpGBT will both be used to achieve good signal characteristics for the high-speed links, while for the command stream the pre-emphasis of the LpGBT driver can be used. The first operation of RD53A chips with twisted pair e-links was successful and demonstrated the twisted pair to be a viable solution, satisfying the LpGBT requirements. Maintaining signal integrity and minimising the cross coupling between the links is critical and more studies with e-links laid on a prototype service cylinder emulating their final arrangement are planned for 2020.

5. Conclusions

A completely new pixel detector is being designed for the CMS Phase 2 Upgrade. The new layout features an extended forward coverage that will also be exploited for luminosity measurements. The critical components of the system are under development. The demonstrator RD53A chip has shown full functionality, while the RD53 design team is preparing for the final CMS pixel chip submission in 2020. The final choice of the sensor technology and the pixel aspect ratio is also planned for 2020 based on results from irradiated sensors to the ultimate fluence. The system architecture has been based on technology choices for low mass, radiation hard and high bandwidth solutions. The first successful power and readout tests have been performed with RD53A modules in serial power chains, readout by prototype e-links.

Many developments are ongoing with important milestones for the project planned for 2020.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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